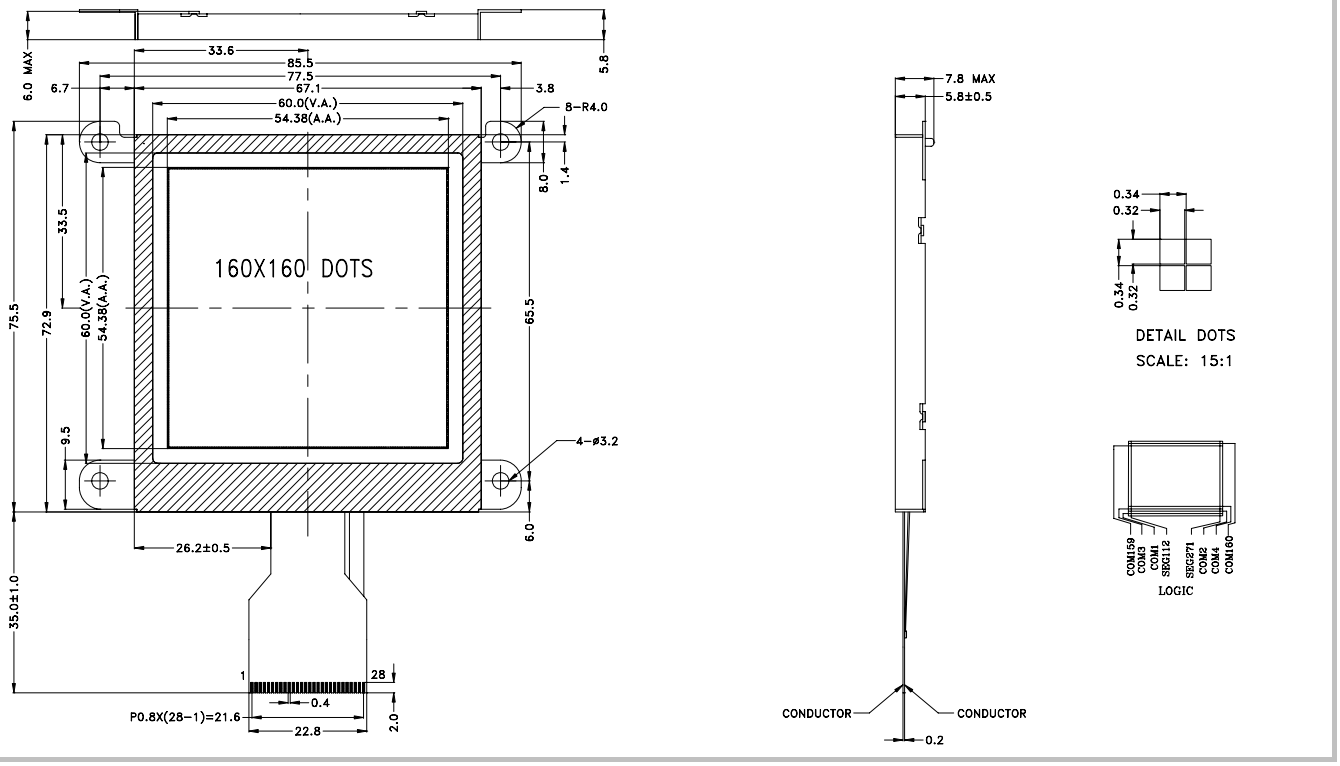
Outline Dimension



Graphic Type

Feature:

1、160x160 dot-matrix
2、FSTN/Transflective/Positive/B-W
3、Backlight: White/side light
4、Operating Temp.: -20℃～+70℃
5、1/160 duty cycle, 1/10 Bias
6、Built-in Controller（UC1698 or equivalent）
7、Viewing angle: 6 o'clock

Absolute Maximum Rating:

Item	Symbol	Standard value			Unit
		M_{IN}	T_{YP}	M_{AX}	
Power supply for logic	V_{DD}-V_{SS}	-0.3	--	+4.0	V
Input voltage	V_I	-0.4	--	V_{DD} +0.5	V

Electrical Characteristic: (VSS=0V, Ta = 25℃)

Parameter	Symbol	Condition	M_{IN}	T_{YP}	M_{AX}	Unit
Supply voltage for logic	V_{DD}	--	3.1	3.3	3.5	V
Supply current for logic	I_{DD}	--	--	1	--	mA
Operating voltage for LCD	V_{LCD}	-20℃	--	--	--	V
		+25℃	--	16.5	--	V
		+70℃	--	--	--	V
Supply voltage for Backlight	V_{BL}	--	--	3.1	--	V
Supply current for Backlight	I_{BL}	--	--	75	--	mA

Interface Pin Connections:

Pin No.	Symbol	Level	Description
1	VLCD	--	High voltage LCD Power Supply. Connect these pins together. Capacitor CL should be connected between VLCD and VSS. In COG applications, keep the ITO trace resistance around 20 Ω.
2	VS+	--	LCD SEG driving voltages. These are the voltage sources to provide SEG driving currents. These voltages are generated internally. Connect capacitors of CBX value between VBX+ and VBX–. Connect a 150 ~ 220nF / 25V capacitor between VS+ and VS-. The resistance of these traces directly affects the driving strength of SEG electrodes and impacts the image of the LCD module. Minimize the trace resistance is critical in achieving high quality image.
3	VS-	--	
4	VB0-	--	
5	VB1-	--	
6	VB1+	--	
7	VB0+	--	
8	VDD	+3.3V	Supply voltage for logic operating.
9	VSS	0V	Ground.
10	TST4	--	Test control. This pin has on-chip pull-up resistor. Leave it open during normal operation. TST4 is also used as one of the high voltage power supply for MTP programming operation. For COG designs, please wire out TST4 with trace resistance between 30~50 Ω.
11	BM0	H/L	"L": 8080/8-bit "H": 6800/8-bit
12	CS	H/L	Chip Select. Chip is selected when CS = "L". When the chip is not selected, D[7:0] will be high impedance.
13	CD	H/L	Selects Control data or Display data for read/write operation. "L": Control data "H": Display data
14	WR1	H/L	WR[1:0] control the read/write operation of the host interface. See section Host Interface for more detail. In parallel mode, the meaning of WR[1:0] depends on whether the interface is in the 6800 mode or the 8080 mode. In serial interface modes, these two pins are not used, connect them to VSS.
15	WR0	H/L	
16	RST	H/L	When RST="L", all control registers are re-initialized by their default states. Since UC1698u has built-in Power-ON reset and software reset commands, RST pin is not required for proper chip operation. An RC Filter has been included on-chip. There is no need for external RC noise filter. When RST is not used, connect the pin to VDD.
17~24	D0~D7	H/L	Bi-directional bus for parallel host interfaces.
25&26	LED+	+3.1V	Power supplay for Back Light.
27&28	LED-	0V	Ground for Back Light.